extending possibilities

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RakunLS1, Qseven SBC module with LS1021A

HW Specification

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table of contents

TABLE OF CONTENTS

table of contents

illustration index

ILLUSTRATION INDEX

index

INDEX OF TABLES

1 GENERAL

1.1 ABOUT THIS DOCUMENT

This document defines the hardware architecture of the RakunLS1 Qseven module.

1.2 REVISION HISTORY

Revision	Date	Notes
1.0	8. June 2015	Initial version
1.1	6. April 2016	Update, cleanup

Table 1.1: Revision history

1.3 ACRONYMS AND ABBREVIATIONS

Acronym	Meaning
ARM	Advanced RISC Machines
BIST	Built In Self Test
CAN	Controller Area Network, type of bus
CE	CE marking, Conformité Européenne
CEC	Consumer Electronics Control, part of HDMI
CD	Carrier Detect
CFG	Configuration
CLK	Clock
COP	Computer Operating Properly, debug interface of MPC8306
CPU	Central Processing Unit
CS	Chip Select
CTS	Clear To Send, UART handshaking signal
DC	Direct Current
DC/DC	Type of power supply
DDR3L	Dual Data Rate, type of Dynamic Random Access Memory
DVI	Digital Visual Interface
EC	Ethernet Controller
ECC	Error Correcting Code
ETH	Ethernet
FTM	Flex Timer Module
FIFO	First-IN, First-Out, memory type

Acronym	Meaning
GB	Giga Byte (1024 MB)
GPIO	General purpose IO
GND	Ground, common reference potential
HDLC	High-Level Data Link Control
HDMI	High-Definition Multimedia Interface
HDTV	High-Definition Television
HPD	Hot Plug Detect
HW	Hardware
I2C	Inter Integrated Circuit, type of bus
I2S	Integrated Inter-chip Sound
IEEE	Institute of Electrical and Electronics Engineers
IO	Input/Output
IRAM	Instruction Random Access Memory, one of MPC8306's internal memories
IRQ	Interrupt ReQuest
JTAG	Joint Test Action Group
KB	Kilo Byte (1024 B)
KV	Kilo Volt (1000V)
LED	Light Emitting Diode
LPCM	Linear Pulse-Code Modulation
LPUART	Low Power UART
MAC	Media Access Control
MB	Mega Byte (1024 KB)
MDI	Media Dependent Interface
MDIO	MII management bus
MII	Media Independent Interface
MMC	Multi Media Card
MISO	Master In Slave Out
MOSI	Master Out Slave In
NAND (Flash)	Type of Flash memory
NC	Not Connected
NOR (Flash)	Type of Flash memory
PCIe	Peripheral Component Interconnect Express, , type of bus
PHY	Physical interface (IC)
PLL	Phase-Locked Loop
PWM	Pulse Width Modulation
RGMII	Reduced Gigabit MII
QE	QUICC Engine
QSPI	Quad SPI, type of bus
QUICC	Quad Integrated Communications Controller
OTG	On The Go
RISC	Reduced Instruction Set Computer

Acronym	Meaning
ROHS	Restriction Of Hazardous Substances
RTS	Request To Send, UART handshaking signal
SATA	Serial AT Attachment, type of bus
SD	Secure Digital
SDHC	Secure Digital High Capacity
SGMII	Serial Gigabit MII
SLC	Single Level Cell, type of NAND memory
SPDIF	Sony/Philips Digital Interface Format
SPI	Serial Peripheral Bus, type of bus
SXGA	Monitor resolution, 1280 x 1024
SW	Software
SWD	Serial Wire Debug, ARM’s debug interface
TDM	Time Division Multiplex
UART	Universal Asynchronous Receiver/Transmitter
UCC	Universal Communications Controller
ULPI	USB digital bus
USB	Universal Serial Bus
WOL	Wake On Lan

Table 1.2: Acronyms

2 INTRODUCTION

2.1 DEVICE OVERVIEW

RakunLS1 is a Single Board Computer based on Freescale's LS1021A processor, member of the QorIQ Layerscape 1 family. It features up to 5000 CoreMarks of CPU power, 1GB DDR3L memory with ECC, 1GB NAND Flash memory, 32MB qSPI NOR flash, 10/100/1000 Ethernet PHY, 4 6Gb/s SerDes Lanes used for SGMII/PCIe/SATA, PWM channels, CAN bus, UARTs etc.

It is in a Qseven form factor and offers interfaces, used in telecom and industrial applications.

It runs Linux operating system.

2.2 FEATURES

All of the below listed I/O interfaces are not available simultaneously. Availability depends on the pinmuxing of the CPU.

CPU

Freescale LS1021A CPU, running at 1GHz.
Dual-core Cortex A7 architecture. 32KB data and 32KB instruction L1 cache per core. 512KB unified L2 cache. Floating point units, NEON co-processor. QorIQ trust architecture.
QUICC Engine uLite block: 32bit RISC controller, 2 UCCs. Supporting HDLC, TDM, UARTs.

Memory

1GB DDR3L memory with ECC. 1600MHz data rate, 32 bit bus. Optional capacities are 256MB, 512MB, 2GB and 4GB (4GB in 0 – 95 degC only).
1GB SLC NAND flash (8 bit bus). Hardware accelerated high speed access with ECC support. Optional capacities are 64MB to 2GB.
Dual 32MB QSPI NOR flash. Optional capacities are 4MB to 256MB, single NOR device is optional also. It is the default boot memory. There are two devices on the bus, boot agent can swap them in case of boot failure.

Ethernet Interfaces

Up to three 10/100/1000 Mbps Ethernet ports, one with PHY on module, two RGMII/SGMII Ethernet ports off module. IEEE 1588 precision clock synchronization.

USB Interface

USB 3.0 Interface with PHY or USB 2.0 OTG interface with PHY.

PCIe Interface

Up to 2 PCIe Gen2 interfaces. Single up to x4, dual up to x2. PCIe ports are shared with SGMII and SATA ports.

SATA Interface

One SATA 3.0 (up to 6Gb/s) interface.

UART Interfaces

Up to six UARTs with FIFO.

Two full featured UARTs with hardware handshaking (16450/16650 compatible) or four standard UARTs without hardware handshaking (Null-modem). Two additional full featured UARTs with hardware handshaking on QE.

CAN Interface

Up to four CAN buses. CAN PHYs are not on module.

QUICC Engine

One RISC, two UCCs available. Each UCC supports HDLC, UART, BISYNC. TDM, transparent.
TDM interfaces with up to 128 channels, each running at 64Kbps. Transparent protocol: 1-bit (serial) data on UCC1, 1- and 4-bit data on UCC3. Custom microcodes available upon request.

Other interfaces

Two I2C buses.
SPI interface with two CS.
ESDHC/MMC/eMMC interface
PWM channels.
I2S, S/PDIF interfaces
GPIOs

Display

HDMI Transmitter ADV7524A onboard. Supports HDTV formats up to 1080p and computer graphics resolutions up to SXGA (1280×1024) at 75Hz. HDMI version 1.4A, CEC.

Power Supply

Single 5.0V DC, +- 5%.
On-board regulators, brown-out detection and watchdog.
Typical power consumption < 4W during full operation.
Power-save modes.

Physical

Physical Dimensions: 70×70 mm, Qseven form factor.
Attachment: Qseven v2.0 230 pin edge connector. Additional mounting holes for reliable attachment.

Environment

Storage: -65ºC to +150ºC
Operation: -40ºC to +85ºC (-25ºC to +85ºC with HDMI transmitter)
Humidity: 5% to 90% Non-Condensing
Electrostatic Discharge Tolerance: 2KV
Pb free, ROHS compliant

Approvals

CE

Operating Systems

Yocto Linux (kernel 3.12.37)

2.3 VARIANTS

Name	Description
AA	Modified Qseven with HDMI, 2.5V GPIOs on LVDS lines, SATA, 3x PCIe **(Default)**
AB	Modified Qseven with HDMI, 2.5V GPIOs on LVDS lines, 4x PCIe
AC	Modified Qseven with HDMI, 3.3V GPIOs on LVDS lines, SATA, 2x PCIe
BC	Modified Qseven with full Quicc Engine, 3.3V GPIOs on LVDS lines, SATA, 2x PCIe
CA	Strict Qseven, SATA, 3x PCIe
CB	Strict Qseven, 4x PCIe
	Other combinations available upon request

Table 2.1: Variants of the board

3 ARCHITECTURE

3.1 BLOCK DIAGRAM

Figure below shows block diagram of the device:

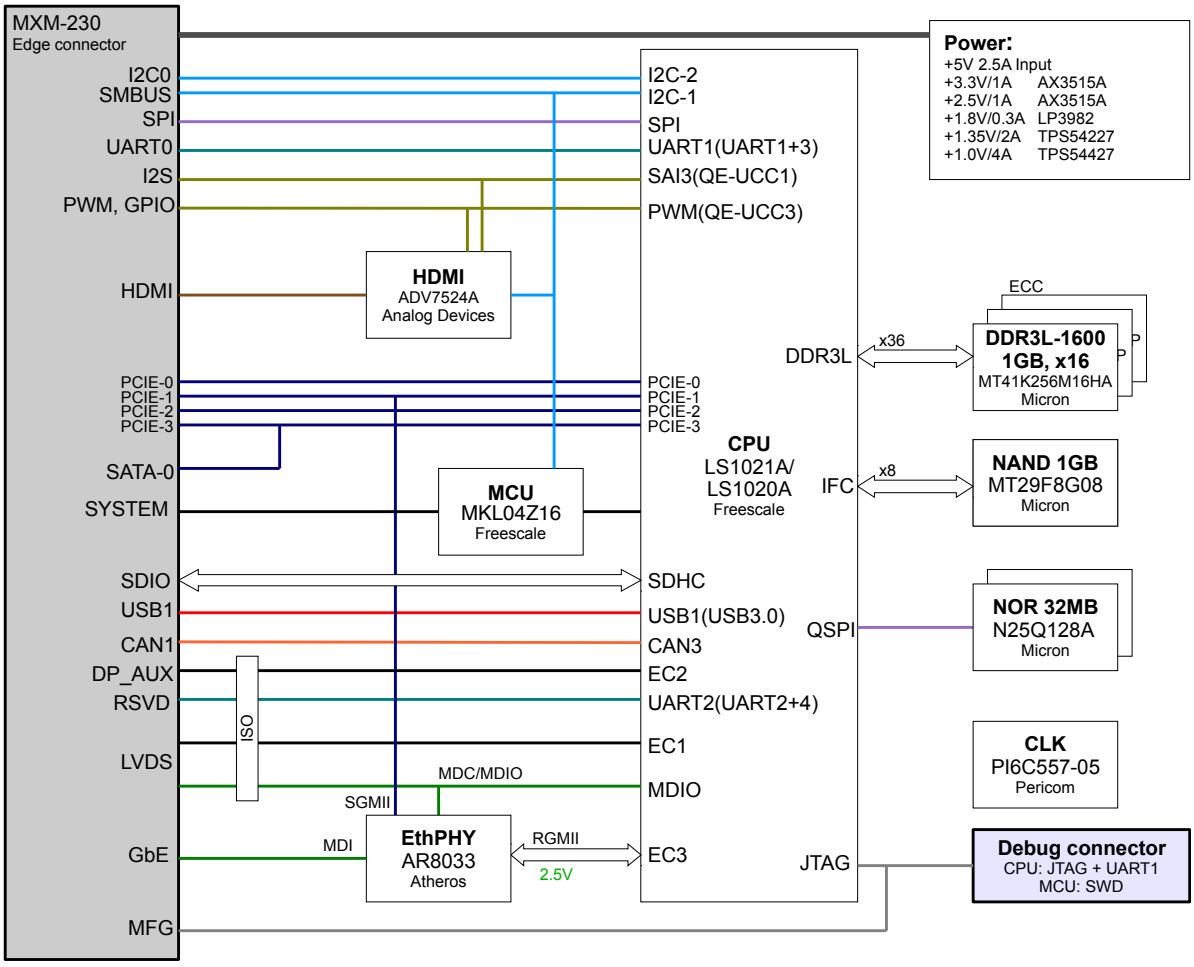

Illustration 3.1: Block diagram

3.2 CPU

CPU used in RakunLS1 is Freescale LS1021A.

LS1021A is a QorIQ integrated multicore processor with two power efficient 1 GHz ARM® Cortex®-A7 cores, each with ECC-protected L1 and L2 cache memories for high reliability and a combined 512KB L2 cache. CPU provides CoreMark. performance of over 5,000 at a power consumption below 3W.

Interfaces of the CPU can be seen on the figure below. Interfaces on this CPU are heavily multiplexed. This document will show the limitations in the following chapters.

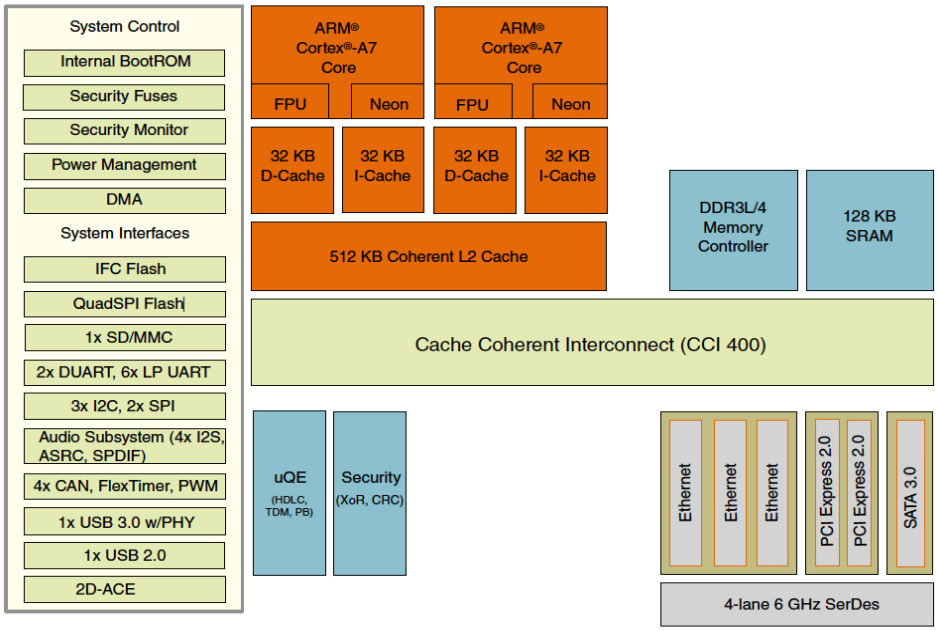

Illustration 3.2: Block diagram of LS1021A

LS1021A includes a QUICC Engine RISC core (QE). QE is a communication coprocessor supporting a variety of communication protocols. Workload can be divided between A7 and QE cores: QE takes care of low levels, A7 cores take care of the high levels. QE normally executes a set of standard Freescale microcodes, covering various communication protocols. However, QE is programmable, therefore it is possible to implement a yet unsupported protocol if required or implement additional A7 offload if performance is an issue.

3.3 MEMORY

3.3.1 VOLATILE

RakunLS1 is equipped with 1GB of DDR3L memory running at 1600MHz data rate. Width of DDR3L bus is 32 bits, which gives peak memory bandwidth 6.4GB/s. Currently design uses Micron MT41K256M16HA-125:E. Several alternatives exist. Design supports DDR3L memory up to 4GB. There are two memory devices on board. Optionally, memory can be ECC protected with the addition of the third device.

Please note that 4GB is currently available in commercial temperature range only (0 – 95 degC).

3.3.2 NON-VOLATILE

There are two non-volatile memories. First is SLC NAND flash memory. It is connected to the CPU with 8 bit bus running at 50MHz. CPU integrates hardware accelerated high speed NAND memory controller with ECC support. By default design uses 1GB device Micron MT29F8G08ADADAH4-IT. Several alternatives exist. Design supports SLC NAND flashes from 64MB to 2 GB.

Second flash is QSPI NOR flash memory. There are two identical QSPI NOR flashes on board. They are logically interchangeable by system logic, thus providing fail-safe redundant boot. Both are connected to QSPI-A bus. Usage of second NOR is optional. QSPI NOR flash is the default boot memory. By default design uses two 32MB devices Micron N25Q128A13E1240F. Several alternatives exist. Design supports QSPI NOR flashes from 4MB to 256MB.

3.4 I/O INTERFACES

RakunLS1 is designed to be as versatile as possible. Limited by onboard peripherals and Qseven pinout, the RakunLS1 design provides as many I/O interfaces to the user (carrier board) as possible.

Due to limited number of pins on the package, CPU uses pinmuxing on its I/O pins. This means several different interfaces share the same pins and can not be used at the same time or in the same application. RakunLS1 design does not limit the usage of multiplexed interfaces, however standard ones are connected to the proper Qseven connector pins.

Standard interfaces, that are included in the Qseven connector pinout, are connected as the Qseven specification 2.0 defines. However, RakunLS1 design does not limit the usage of these to their default function. For example, CPU's SDHC interface is connected to the SD pins of Qseven connector. But these pins can also be used as LPUARTs or GPIOs, if SDHC interface is not required.

Other CPU I/O interfaces are connected to the Qseven 2.0 edge connector. All available interfaces are:

- 10/100/1000 Ethernet (Qualcomm-Atheros AR8033)
- 2x RGMII
- 2x SGMII
- MDIO
- 4x CAN
- SATA 3.0
- 4x PCIe
- 4x I2S
- 3x FTM (timers I/O, PWM); 26 PWM channels altogether
- 2x USB; One with integrated PHY (usable as USB 3.0 or as USB 2.0 OTG), second USB 2.0 - ULPI bus
- 8x UARTs
- SPI
- HDMI
- TDM
- HDLC
- SPDIF
- 2x I2C
- SDHC
- GPIOs

Please note they are not all available simultaneously.

RakunLS1 implements one 10/100/1000 Mb/s Ethernet interface on board. Ethernet PHY Qualcomm-Atheros AR8033 is connected to the CPU with RGMII or SGMII bus, depending on a variant.

3.4.1 OPTIONAL DEVIATION FROM QSEVEN SPECIFICATION

RakunLS1 can be used as a standard Qseven 2.0 module or as a modified one. Qseven specification defines group of pins that are used for LVDS flat panel display connection (chapter 3.1.8 in Qseven Specification 2.0). LS1021A CPU does not provide such interface. RakunLS1 uses these pins for other interfaces, that are not present in standard Qseven pinout. With this deviation from Qseven 2.0 specification, the module becomes more usable in embedded applications.

All signals, that are not following the Qseven 2.0 specification, can be isolated with 0R resistors. With such an isolation, RakunLS1 becomes fully Qseven 2.0 compliant, but without additional interfaces. Interfaces, provided by RakunLS1 on LVDS pin group of Qseven, are:

- EC1-RGMII/MII
- EC2-RGMII/MII
- CAN1

- CAN2
- CAN4
- I2S_1
- I2S_2
- FTM1
- FTM2
- UART2
- UART4
- MII management bus (MDIO)

Please note that all of them can not be used simultaneously due to pinmuxing. Availability is presented in the next chapter.

3.4.2 SUMMARY OF I/O INTERFACES

Summary of the I/O interfaces is presented in the table below. Interfaces in the same horizontal share common CPU pins and/or Qseven pins and cannot be used simultaneously! For example, if CAN1 is used, EC1-RGMII is not available.

EC2-RGMII	CAN3	GPIO		USB2-ULPI	FTM2	
	CAN4					
EC3-RGMII	PTP	GPIO		USB2-ULPI	FTM3	RMII
UART1-FULL	UART1-NM	GPIO				
	UART2-NM	GPIO	LPUART1		SPI	
UART2-FULL	UART3-NM	GPIO	LPUART2			HDMI
	UART4-NM		LPUART1	LPUART4		
QE-UCC1	I2S_3	GPIO		FTM4		HDMI
QE-UCC3	I2S_4	GPIO	SPDIF	FTM4		
I2C_1						
I2C_2	SD WP,CD	GPIO	QE STROBE			
SDHC	LPUART3	GPIO				
	LPUART6					
	USB1 PWR					
SPI						
USB1	USB1:3.0	USB1:2.0 OTG				
MDIO		GPIO				
ETHERNET						

Table 3.1: Summary of I/O interfaces

For more details, please check the LS1021A documentation or Pinmuxing spreadsheet.

3.4.3 SUMMARY OF SERDES INTERFACES

Similarly as above, SerDes lanes are also multiplexed offering variety of possibilities. The following configurations are supported:

Option	Lane 0	Lane 1	Lane 2	Lane 3
0x00	PCIe1(x4)			
0x80	PCIe1(x2)		PCIe2(x2)	
0x10	PCIe1(x1)	SATA1	PCIe2(x2)	
0x20	PCIe1(x1)	SGMII1	PCIe2(x1)	SGMII2
0x30	PCIe1(x1)	SATA1	SGMII1	SGMII2
0x50	PCIe1(x2)		PCIe2(x1)	SGMII2
0x60	PCIe1(x2)		SGMII1	SGMII2
0x70 (default)	**PCIe1(x1)**	**SATA1**	**PCIe2(x1)**	**SGMII2**

Table 3.2: Summary of SerDes interfaces

CPU comprises four SerDes lanes. PCIe, SATA and SGMII interfaces are available on these lanes, as shown in table above. Interconnects between CPU and Qseven edge connector is shown in figure below. Two of them are connected directly to edge connector. Other two can be connected directly or used as a SATA interface or for a SGMII connection to the onboard Ethernet PHY. Default interconnects are shown with continuous line, optional with dashed line.

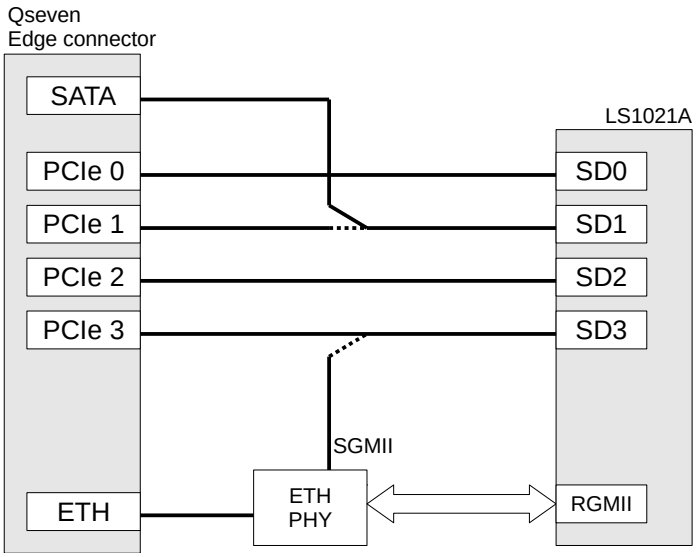

Illustration 3.3: SerDes interconnects

3.5 DISPLAY INTERFACE

Video HDMI interface is implemented with low power HDMI transmitter Analog Devices ADM7524A. Features:

- CEC controller and expanded message buffer
- HDMI Version 1.4a features supported
- Compatible with DVI 1.0
- Optional embedded HDCP keys to support HDCP 1.3
- 150 MHz operation supports all video and graphics resolutions from 480i to 1080p (or SXGA)

- Programmable 2-way color-space converter
- Supports ITU656-based embedded syncs
- Automatic input video format timing detection (CEA-861E)
- 2-channel, uncompressed LPCM I2S audio up to 192 kHz
- On-chip MPU with I2C master to perform EDID reading and HDCP operations; reports HDMI events through interrupts
- and registers
- 5 V tolerant I2C and HPD I/Os
- 5 V generator for Hot Plug detection in portable applications

HDMI transceiver uses CPU's SAI1 interface for audio. Pins of this interface are shared (multiplexed) with EC1-RGMII bus, used for onboard Ethernet PHY connection. HDMI audio is therefore available in variants with SGMII connection to the onboard PHY only.

3.6 SYSTEM LOGIC

Due to high integration of LS1021A, there is little system logic required on the RakunLS1. To spare CPU GPIOs for more important I/O interfaces, a low cost Kinetis KL04 MCU is used for controlling the Qseven system signals and other system tasks. Features of the system supervisor MCU:

- Power-on sequence generation
- Power rails voltage measurement/supervision
- CPU reset generation
- On-board temperature sensing
- CPU-MCU communication: I2C bus and IRQ lines
- Qseven system signals control (reset button, sleep button, SMB alert, WDT trig, PWR button, WDOUT, SUS_S3#)
- CPU bootstrapping & QSPI Flash selection
- CPU power management (wakeup from sleep modes)
- LED control

For debugging and initial loading (initial flash programming) purposes there are two debug connectors on the board. They provide SWD for MCU, JTAG/COP for CPU, debug UART (console) interfaces, suitable for both engineering debug and manufacturing testbed.

3.7 RESET SUBSYSTEM

Main reset signal in the system is generated with KL04 MCU, who serves as supervisor of the system. Signal coming from it is joined with the reset signal coming from the debugger to enable debugger operation.

Peripheral resets are connected to the CPU's GPIO ports. They are activated together with the main reset and later controlled with software.

3.7.1 PERIPHERAL RESET SIGNALS

Table shows peripheral reset signals:

Device	Signal	Active	Control	Description
Ethernet PHY	ETHPHY_RST#	Low	GPIO2_15	Reset of Ethernet PHY AR8033
PCIe subsystem	PCIE_RST#	Low	GPIO2_13	Reset of PCIe; Connected to Qseven connector

Table 3.3: Peripheral reset signals

3.8 CLOCKING SUBSYSTEM

RakunLS1 uses highly optimized clock subsystem. For main CPU clock one of PCIe clocks is used. These clocks are generated with dedicated PCIe clock generator/buffer, who generates 100MHz clock for PCIe subsystem. Two clock lanes are needed for CPU SerDes block and one for the Qseven PCIe clock reference. PCIe clock generator uses dedicated 25MHz quartz crystal.

From its input clock, CPU generates most of the clocks needed for the system internally. This includes internal platform clock, core clocks, DDR3L clock, clocks for all other peripheries except RGMII buses. Those buses require external 125MHz reference clock. For RGMII1, which is connected to the onboard Ethernet PHY, this clock is derived from the PHY itself, which has a general purpose clock output. Ethernet PHY uses dedicated 25MHz quartz crystal.

3.8.1 CPU PLLS

LS1021A on RakunLS1 uses single 100MHz input clock for its internal PLL clock generators. They are platform, core, DDR PLLs. PLLs are set up from reset configuration word.

CPU clock configuration is as follows:

Name	Speed
A7 Cores	1GHz (Default)
DDR3L	800MHz (1600MHz data rate)
Platform	400MHz
QE	400MHz

Table 3.4: CPU frequencies

Both cores run at the same frequency. Dynamic Frequency scaling of the core frequency is supported.

3.9 POWER SUPPLY SUBSYSTEM

Board is supplied with main power supply +5V +/-5%, coming from the Qseven connector. This voltage is converted into several different voltages that are needed on the board. DC/DC converters with high efficiency are used for conversion of high load rails and linear regulators for light load rails. Power-on is controlled with supervisor and power control from the carrier board. Power on RakunLS1 is applied in multiple stages:

Stage 1:
3.3V DCDC starts when 5V power is applied and PWGIN signal is active. Supervisor MCU is supplied from 3.3V DCDC directly, it starts immediately and gains control over the module.

Stage 2:
At active PWR_EN signal power-on sequence starts. Supervisor turns on 3.3V MOSFET switch (enabling 3.3V power to the rest of the module), 2.5V DCDC and two 1.8V linear regulators for HDMI and CPU.

Stage 3:
3.3V voltage rail enables 1.0V DCDC.

Stage 4:
3.3V voltage rail with RC delay enables 1.35V DCDC.

Stage 5:
After all power rails are active, supervisor checks if voltages are in required tolerances. If all is OK, supervisor deactivates CPU reset. If any of the power supplies fail, it reports failure via LED blink.

3.10 SECURITY

LS1021A supports QorIQ trust architecture, secure boot, and ARM TrustZone® technologies. Use of the Trust Architecture features is dependent on programming fuses in the Security Fuse Processor (SFP).

To program SFP fuses, the user is required to supply 1.8 V to the TA_PROG_SFP pin. TA_PROG_SFP should only be powered for the duration of the fuse programming cycle, with a per device limit of two fuse programming cycles. All other times, TA_PROG_SFP should be connected to GND. TA_PROG_SFP is available on connector J2.

The details of the Trust Architecture and SFP can be found in the LS1021A reference manual.

3.11 BOOT

LS1021A CPU is initialized using two complementary methods: latching reset configuration bootstrap signals and loading the reset configuration word.

3.11.1 RESET CONFIGURATION SIGNALS

The device samples reset configuration signals CFG_RCW_SRC(0:8) during the assertion of the PORESET signal. These signals define the source (interface and memory type) which the reset configuration word and boot code is loaded from.

RakunLS1 supports two boot sources, QSPI NOR flash and SD card. Selection between the two is made by bootstrapping the SLP_BTN# system signal during reset.

CFG_RST(0:8)	Meaning	SLP_BTN# bootstrap
001000100	Boot from QSPI flash (**Default**)	Open or ‘1’
001000000	Boot from SD/MMC	‘0’
TBD	Boot from NAND (Possible, but optional upon request)	---

Table 3.5: Boot source selection

After configuration word is loaded and PLLs are locked, CPU starts fetching code from the same location.

3.11.2 RESET CONFIGURATION WORD

Reset configuration word is a 512 bit word which defines all required boot parameters and initial CPU configuration, such as: internal PLLs ratios, clock sources and frequencies, pin multiplexing etc.

Below is example of configuration word for AA variant of the board, boot from SD card.

Address	W0	W1	W2	W3
00000000	0608000a	00000000	00000000	00000000
00000010	10000000	08007920	60025a00	21046000
00000020	00000000	00000000	00000000	20038700
00000030	20024900	001b7340	00000000	00000000

Table 3.6: Boot source selection

4 INTERRUPT SIGNALS

LS1021A receives interrupt requests from the periphery on RakunLS1 and carrier board. Interrupt signals are divided into dedicated IRQ signals and GPIO signals. Any GPIO on LS1021A can be configured as an interrupt request input.

Dedicated interrupt signals on the RakunLS1 are listed below:

IRQ	Signal	Description
IRQ0	ETHPHY_WOL#	Wake On LAN IRQ from Ethernet PHY AR8033
IRQ1	ETHPHY_INT#	IRQ from Ethernet PHY AR8033
IRQ2	IRQ_HDMI#	IRQ from HDMI transmitter AD7524A
GPIO1	Any GPIO	Application specific; All GPIO interrupts are OR-ed together.

Table 4.1: Interrupt signals

Interrupt requests from GPIO signals depend on application usage. They will come from carrier board. RakunLS1 module itself does not use GPIO interrupts.

5 I/O INTERFACES

5.1 QSEVEN SYSTEM SIGNALS

Qseven standard requires some system signals that take care of possible external management of the board. Some of the signals are mandatory, some are optional. RakunLS1 has mandatory signals implemented only. These signals are controlled by onboard MCU.

Signals of Qseven system interface:

KE1 Pin	Signal	Direct-ion	Function	Note
18	SUS_S3#	Out	S3 State: This signal shuts off power to all runtime system components that are not maintained during S3 (Suspend to Ram), S4 or S5 states.	PU
20	PWRBTN#	In	Power Button. Low active power button input. This signal is triggered on the falling edge.	PU
21	SLP_BTN#	In	Sleep button. Low active signal used by the ACPI operating system to transition the system into sleep state or to wake it up again. This signal is triggered on falling edge.	PU
26	PWGIN	In	High active input for the module indicates that all power rails located on the carrier board are ready for use.	PU, 5V
28	RSTBTN#	In	Reset button input. This input may be driven active low by an external circuitry to reset the module.	PU
70	WDTRIG#	In	Watchdog trigger signal. This signal restarts the watchdog timer of the module on the falling edge of a low active pulse.	PU
72	WDOUT	Out	Watchdog event indicator. High active output used for signaling a missing watchdog trigger. Will be deasserted by software, system reset or a system power down.	

Table 5.1: Qseven System signals

5.2 ETHERNET (ETH0)

10/100/1000 Mb/s Ethernet interface on the RakunLS1 is implemented with Qualcomm Atheros AR8033 Ethernet PHY. It is connected to the EC1 controller in LS1021A with RGMII and MDIO buses.

After put out of the reset, PHY starts with the following default settings:

- Speed 1000M
- Full duplex
- Auto-negotiation enabled
- Power-down disabled
- MDIO address 0x07

Transformer and ESD protection needs to be implemented on a base board.

5.2.1 MDI INTERFACE

Signals of Ethernet interface:

KE1 Pin	Signal	Direction	Function	Note
12	ETH_MDI0+	Bidir	Media Independent Interface, positive of pair 0	
10	ETH_MDI0-	Bidir	Media Independent Interface, negative of pair 0	
11	ETH_MDI1+	Bidir	Media Independent Interface, positive of pair 1	
9	ETH_MDI1-	Bidir	Media Independent Interface, negative of pair 1	
6	ETH_MDI2+	Bidir	Media Independent Interface, positive of pair 2	
4	ETH_MDI2-	Bidir	Media Independent Interface, negative of pair 2	
5	ETH_MDI3+	Bidir	Media Independent Interface, positive of pair 3	
3	ETH_MDI3-	Bidir	Media Independent Interface, negative of pair 3	

Table 5.2: Ethernet signals

MDI signals are not isolated from the connector KE1. Ethernet transformer and ESD protection needs to be present on the carrier.

5.2.2 ETHERNET LEDS

Signals of Ethernet LEDs:

KE1 Pin	Signal	Direction	Function	Note
7	LINK100#	Out	LED for Speed 100Mb/s indication	Active low
8	LINK1000#	Out	LED for Speed 1000Mb/s indication	Active high
14	ACT#	Out	LED for Activity indication	Active low

Table 5.3: Ethernet LEDs

Default behavior of LEDs:

Signal	On	Off	Blinking
LINK100#	Link established, speed 100Mb/s	No link on 100Mb/s	
LINK1000#	Link established, speed 1000Mb/s	No link on 1000Mb/s	
ACT#	Traffic	No traffic	Traffic

Table 5.4: Ethernet LEDs

Its behavior can be changed with software. Consult AR8033 data sheet. Please note polarization of LEDS are different.

5.3 USB 3.0

USB3.0 interface supports super-speed (SS), high-speed (HS), full-speed (FS) and low-speed (LS) operations. In USB2.0 mode, OTG is supported.

- USB 3.0 PHY, LINK, and MAC layers
- USB 2.0 PHY and MAC layers
- The upper layer is common for USB 2.0 and USB 3.0 operation. This has the Bus Interface, Buffer Management block, List Processor for scheduling, and Control and Status Register (CSR) functions.

ESD protection needs to be implemented on a base board. There is additional USB2.0 OTG interface available, but without integrated PHY. ULPI bus is shared with EC2 and EC3 pins.

Signals of USB3.0 interface:

KE1 Pin	Signal	Direction	Function	Note
83	USB1_TX+	Out	USB3.0 super speed transmit positive data	
81	USB1_TX-	Out	USB3.0 super speed transmit negative data	
84	USB1_RX+	In	USB3.0 super speed receive positive data	
82	USB1_RX-	In	USB3.0 super speed receive negative data	
95	USB1_D+	Bidir	USB2.0 receive positive data	
93	USB1_D-	Bidir	USB2.0 receive negative data	
92	USB1_ID	Bidir	USB2.0 OTG ID signal	
91	USB1_VBUS	In	USB VBUS power	
86	USB1_PWRFAULT	In	USB over current detect input	Active low
56	USB1_DRVBUS	Out	USB power enable output	Active high

Table 5.5: USB signals

5.4 PCIE

RakunLS1 comprises two PCIe 3.0 interfaces, available on 4 5GHz SerDes lanes. These lanes are shared with SATA and SGMII interfaces also. Configuration of SerDes lanes needs to be defined in configuration word. Possible configurations are as follows:

SRDS_PRTCL_S1(128:135)	A	B	C	D
0x00	PCIE1 (x4)			
0x80	PCIE1 (x2)		PCIE2 (x2)	
0x10	PCIE1 (x1)	SATA0	PCIE2 (x2)	
0x20	PCIE1 (x1)	SGMII1	PCIE2 (x1)	SGMII2
0x30	PCIE1 (x1)	SATA0	SGMII1	SGMII2
0x40	PCIE1 (x2)		SATA0	SGMII2
0x50	PCIE1 (x2)		PCIE2 (x1)	SGMII2
0x60	PCIE1 (x2)		SGMII1	SGMII2
0x70	PCIE1 (x1)	SATA0	PCIE2 (x1)	SGMII2

Table 5.6: SerDes lanes configurations

Note: Usable configurations depend on HW variant of the board! See figure 3.3.

Signals of PCIe interface:

KE1 Pin	Signal	Direction	Function	Note
179	PCIE0_TX+	Out	PCIe0 transmit positive	
181	PCIE0_TX-	Out	PCIe0 transmit negative	
180	PCIE0_RX+	In	PCIe0 receive positive	
182	PCIE0_RX-	In	PCIe0 receive negative	
173	PCIE1_TX+	Out	PCIe1 transmit positive	SATA
175	PCIE1_TX-	Out	PCIe1 transmit negative	SATA
174	PCIE1_RX+	In	PCIe1 receive positive	SATA
176	PCIE1_RX-	In	PCIe1 receive negative	SATA
167	PCIE2_TX+	Out	PCIe2 transmit positive	
169	PCIE2_TX-	Out	PCIe2 transmit negative	
168	PCIE2_RX+	In	PCIe2 receive positive	
170	PCIE2_RX-	In	PCIe2 receive negative	
161	PCIE3_TX+	Out	PCIe3 transmit positive	ETH PHY SGMII
163	PCIE3_TX-	Out	PCIe3 transmit negative	ETH PHY SGMII
162	PCIE3_RX+	In	PCIe3 receive positive	ETH PHY SGMII
164	PCIE3_RX-	In	PCIe3 receive negative	ETH PHY SGMII
155	PCIE_CLK_REF+	Out	PCIe Reference positive clock	
157	PCIE_CLK_REF-	Out	PCIe Reference negative clock	
158	PCIE_RST#	Out	PCIe system reset output	

Table 5.7: PCIe signals

5.5 SATA

There is one SATA interface on board. It is connected to the Qseven SATA0 interface. SATA controller is integrated in the CPU. It includes the following features:

- Complies with the serial ATA 3.0 specification and the AHCI 1.3 specification
- Contains a high-speed descriptor-based DMA controller
- Speeds of 1.5 Gbps (first-generation SATA), 3 Gbps (second-generation SATA) and 6 Gbps (third-generation SATA)
- FIS-based switching
- Advanced technology attachment packet interface (ATAPI) devices
- Native command queuing (NCQ) commands
- Port multiplier operation
- Asynchronous notification
- SATA BIST mode

Signals of SATA interface:

KE1 Pin	Signal	Direction	Function	Note
29	SATA_TX+	Out	SATA Interface, positive transmit	
31	SATA_TX-	Out	SATA Interface, negative transmit	
35	SATA_RX+	In	SATA Interface, positive receive	
37	SATA_RX-	In	SATA Interface, negative receive	

Table 5.8: SATA signals

This interface is internally connected to SerDes Lane 1. This connection is done in HW and depends on variant of the board. See variants in chapter 2.3. When SATA interface is present, Lane 1 in PCIe interface is not available. See chapter 3.3.3.

5.6 SD/MMC

SD/MMC interface is used for connecting the SD, MMC and eMMC cards/devices. There are several interfaces available on the SD group of pins: SD, LPUART, GPIO. They share pins of the CPU, therefore they can not be used simultaneously. Interface needs to be defined in configuration word. They are defined in groups, not individually. For more information, consult LS1021RM [1].

Signals of SD/MMC interface:

KE1 Pin	Signal	Direction	Function	Note
42	SD_CLK LPUART3_CTS# LPUART6_SIN GPIO2_09	Out In In Bidir	SD clock LPUART3 Clear To Send LPUART6 receive data GPIO signal	PU 10K
45	SD_CMD LPUART3_SOUT GPIO2_04	Out Out Bidir	SD command LPUART3 transmit data GPIO signal	PU 10K
49	SD_DATA0 LPUART3_SIN GPIO2_05	Bidir In Bidir	SD data LPUART3 receive data GPIO signal	PU 10K
48	SD_DATA1 LPUART2_RTS# LPUART5_SOUT GPIO2_06	Bidir Out Out Bidir	SD data LPUART2 Request To Send LPUART5 transmit data GPIO signal	PU 10K
51	SD_DATA2 LPUART2_CTS# LPUART5_SIN GPIO2_07	Bidir In In Bidir	SD data LPUART2 Clear To Send LPUART5 receive data GPIO signal	PU 10K
50	SD_DATA3 LPUART3_RTS# LPUART6_SOUT GPIO2_08	Bidir Out Out Bidir	SD data LPUART3 Request To Send LPUART6 transmit data GPIO signal	PU 10K
53	SD_DATA4 GPIO4_23	Bidir Bidir	SD data GPIO signal	PU 10K
52	SD_DATA5 GPIO4_24	Bidir Bidir	SD data GPIO signal	PU 10K
55	SD_DATA6 GPIO4_25	Bidir Bidir	SD data GPIO signal	PU 10K
54	SD_DATA7 GPIO4_26	Bidir Bidir	SD data GPIO signal	PU 10K
43	SD_CD#	In	SD card detect, active low Available on request, shared with I2C_2	Not connected
46	SD_WP	In	SD write protect, active high Available on request, shared with I2C_2	Not connected

Table 5.9: SD/MMC signals

5.7 UART

There are several interfaces available on the UART group of pins: UART, LPUART, GPIO. They share pins of the CPU, therefore they can not be used simultaneously. Interface needs to be defined in configuration word. There are several configurations of UART/LPUART/GPIOs possible. For more information, consult LS1021RM [1].

Signals of UART interface:

KE1 Pin	Signal	Direction	Function	Note
177	UART1_SIN GPIO1_17	In Bidir	UART1 receive data GPIO signal	PU 10K
171	UART1_SOUT GPIO1_15	Out Bidir	UART1 transmit data GPIO signal	
178	UART1_CTS# UART3_SIN LPUART2_SIN GPIO1_21	In In In Bidir	UART1 Clear To Send UART3 receive data LPUART2 receive data GPIO signal	
172	UART1_RTS# UART3_SOUT LPUART2_SOUT GPIO1_19	Out Out Out Bidir	UART1 Request To Send UART3 transmit data LPUART2 transmit data GPIO signal	
146	UART2_SIN LPUART1_SIN GPIO1_18	In In Bidir	UART2 receive data LPUART1 receive data GPIO signal	PU 10K
144	UART2_SOUT LPUART1_SOUT GPIO1_16	Out Out Bidir	UART2 transmit data LPUART1 transmit data GPIO signal	
134	UART2_CTS# UART4_SIN LPUART1_CTS# LPUART4_SIN GPIO1_22	In In In In Bidir	UART2 Clear To Send UART4 receive data LPUART1 Clear To Send LPUART4 receive data GPIO signal	
132	UART2_RTS# UART4_SOUT LPUART1_RTS# LPUART4_SOUT GPIO1_20	Out Out Out Out Bidir	UART2 Request To Send UART4 transmit data LPUART1 Request To Send LPUART4 transmit data GPIO signal	

Table 5.10: UART signals

5.8 I2C_1

Signals of I2C_1 interface:

KE1 Pin	Signal	Direction	Function	Note
60	I2C1_SCL	Bidir	I2C clock	PU 1K
62	I2C1_SDA	Bidir	I2C data	PU 1K
64	SMB_ALERT#	In	SMB interrupt	PU 4.7K

Table 5.11: I2C_1 signals

5.9 I2C_2

There are several interfaces available on the I2C group of pins: I2C_2, SD control, QE, GPIO. They share pins of the CPU, therefore they can not be used simultaneously. Interface needs to be defined in configuration word. They are defined in groups, not individually. For more information, consult LS1021RM [1].

Signals of I2C_2 interface:

KE1 Pin	Signal	Direction	Function	Note
66	I2C2_SCL QE_SI1_STROBE[0] GPIO4_27 SDHC_CD_B	Bidir In Bidir In	I2C clock QE strobe 0 GPIO signal SD card detect	PU 1K
68	I2C2_SDA QE_SI1_STROBE[1] GPIO4_28 SDHC_WP	Bidir In Bidir In	I2C data QE strobe 1 GPIO signal SD write protect	PU 1K

Table 5.12: I2C_2 signals

5.10 SPI

SPI interface is available on the SPI section of Qseven edge connector KE1. It is used for connecting external devices to the CPU. There is no SPI device connected onboard the module. Features:

- Full duplex, 3-wire synchronous transfers. DMA support
- Master mode, Slave mode
- 2 Chip select signals
- Programmable serial frame size 4 – 16bits
- Max. clock frequency 50MHz (Baud rate 25Mb/s). Clock with programmable polarity and phase.

Signals of the SPI interface:

KE1 Pin	Signal	Direction	Function	Note
200	SPI_CS0#	Out	SPI select 0	PU 4.7K
202	SPI_CS1#	Out	SPI select 1	
203	SPI_CLK	Out	SPI clock	PU 4.7K
199	SPI_MOSI	Out	SPI data out	PD 4.7K
201	SPI_MISO	In	SPI data in	PU 4.7K

Table 5.13: SPI signals

5.11 MII MANAGEMENT

Signals of MDIO interface:

KE1 Pin	Signal	Direction	Function	Note
131	MDC_OUT	Out	MDC	PU 1K
133	MDIO_OUT	Bidir	MDIO (Pull-up resistor is on module)	PU 1K

Table 5.14: MIIM signals

5.12 RGMII EC2

There are several interfaces available on the RGMII EC2 group of pins: RGMI-EC2, CAN, USB ULPI bus, PWM, GPIO. They share pins of the CPU, therefore they can not be used simultaneously. Interface needs to be defined in configuration word. They are defined in groups, not individually (e.g. CAN bus takes over the complete interface, even that 4 pins are used only). For more information, consult LS1021RM [1]. This interface is connected to Qseven LVDS pins. All signals can be isolated by means of serial resistors.

Signals of RGMII EC2 interface:

KE1 Pin	Signal	Direction	Function	Note
127	EC2_TXD3 CAN4_TX USB2_D7 FTM2_CH5 GPIO3_15	Out Out Bidir Bidir Bidir	RGMII transmit data 3 CAN4 transmit data USB2 ULPI data bit 7 FTM2 channel 5 input/output GPIO signal	
129	EC2_TXD2 CAN3_TX USB2_D6 FTM2_CH7 GPIO3_16	Out Out Bidir Bidir Bidir	RGMII transmit data 2 CAN3 transmit data USB2 ULPI data bit 6 FTM2 channel 7 input/output GPIO signal	
125	EC2_TXD1 USB2_D5 FTM2_CH3 GPIO3_17	Out Bidir Bidir Bidir	RGMII transmit data 1 USB2 ULPI data bit 5 FTM2 channel 3 input/output GPIO signal	
123	EC2_TXD0 USB2_D4 FTM2_CH2 GPIO3_18	Out Bidir Bidir Bidir	RGMII transmit data 0 USB2 ULPI data bit 4 FTM2 channel 2 input/output GPIO signal	
115	EC2_TX_EN USB2_STP FTM2_FAULT GPIO3_19	Out Out In Bidir	RGMII transmit enable USB2 ULPI stop FTM2 Fault input GPIO signal	
119	EC2_GTX_CLK USB2_CLK FTM2_EXTCLK GPIO3_20	Out In In Bidir	RGMII transmit clock USB2 ULPI clock FTM2 external clock GPIO signal	
121	EC2_GTX_CLK125 USB2_PWRFAULT GPIO3_21	In In Bidir	RGMII 125MHz clock USB2 over current detection GPIO signal	
116	EC2_RXD3 CAN4_RX USB2_D3 FTM2_CH4 GPIO3_22	In In Bidir Bidir Bidir	RGMII receive data 3 CAN4 receive data USB2 ULPI data bit 3 FTM2 channel 4 input/output GPIO signal	
130	EC2_RXD2 CAN3_RX USB2_D2 FTM2_CH6 GPIO3_23	In In Bidir Bidir Bidir	RGMII receive data 2 CAN3 receive data USB2 ULPI data bit 2 FTM2 channel 6 input/output GPIO signal	
114	EC2_RXD1 USB2_D1 FTM2_CH1 GPIO3_24	In Bidir Bidir Bidir	RGMII receive data 1 USB2 ULPI data bit 1 FTM2 channel 1 input/output GPIO signal	
112	EC2_RXD0 USB2_D0 FTM2_CH0 GPIO3_25	In Bidir Bidir Bidir	RGMII receive data 0 USB2 ULPI data bit 0 FTM2 channel 0 input/output GPIO signal	
124	EC2_RX_CLK USB2_DIR FTM2_QD_PHA GPIO3_26	In In In Bidir	RGMII receive clock USB2 ULPI direction FTM2 quadrature decoder phase A input GPIO signal	
110	EC2_RX_DV USB2_NXT FTM2_QD_PHB	In Bidir In	RGMII receive data valid USB2 ULPI next data FTM2 quadrature decoder phase B input	

KE1 Pin	Signal	Direction	Function	Note
	GPIO3_27	Bidir	GPIO signal	

Table 5.15: RGMII EC2 signals

5.13 RGMII EC3

There are several interfaces available on the RGMII EC3 group of pins: RGMI-EC3, PTP, USB ULPI bus, PWM, GPIO. They share pins of the CPU, therefore they can not be used simultaneously. Interface needs to be defined in configuration word. They are defined in groups, not individually (e.g. USB bus takes over the complete interface, even that 1 pin is used only). For more information, consult LS1021RM [1]. This interface is connected to Qseven LVDS pins. All signals can be isolated by means of serial resistors.

Signals of RGMII EC3 interface:

KE1 Pin	Signal	Direction	Function	Note
113	EC3_TXD3 TSEC_1588_ALARM_OUT2 FTM3_CH7 GPIO3_28	Out Out Bidir Bidir	RGMII transmit data 3 PTP alarm signal 2 FTM3 channel 7 input/output GPIO signal	
111	EC3_TXD2 TSEC_1588_ALARM_OUT1 FTM3_CH6 GPIO3_29	Out Out Bidir Bidir	RGMII transmit data 2 PTP alarm signal 1 FTM3 channel 6 input/output GPIO signal	
109	EC3_TXD1 TSEC_1588_CLK_OUT FTM3_CH5 GPIO3_30	Out Out Bidir Bidir	RGMII transmit data 1 PTP clock output FTM3 channel 5 input/output GPIO signal	
107	EC3_TXD0 TSEC_1588_PULSE_OUT2 FTM3_CH4 GPIO3_31	Out Out Bidir Bidir	RGMII transmit data 0 PTP pulse signal 2 FTM3 channel 4 input/output GPIO signal	
103	EC3_TX_EN FTM3_CH1 GPIO4_00	Out Bidir Bidir	RGMII transmit enable FTM3 channel 1 input/output GPIO signal	
105	EC3_GTX_CLK FTM3_CH0 GPIO4_01	Out Bidir Bidir	RGMII transmit clock FTM3 channel 0 input/output GPIO signal	
99	EC3_GTX_CLK125 USB2_DRVVBUS GPIO4_02	In Out Bidir	RGMII 125MHz clock USB2 enable bus power supply GPIO signal	
106	EC3_RXD3 FTM3_FAULT GPIO4_03	In In Bidir	RGMII receive data 3 FTM3 fault signal GPIO signal	
104	EC3_RXD2 FTM3_EXTCLK GPIO4_04	In In Bidir	RGMII receive data 2 FTM3 external clock GPIO signal	
102	EC3_RXD1 TSEC_1588_PULSE_OUT1 FTM3_CH3 GPIO4_05	In Out Bidir Bidir	RGMII receive data 1 PTP pulse signal 1 FTM3 channel 3 input/output GPIO signal	

KE1 Pin	Signal	Direction	Function	Note
100	EC3_RXD0 TSEC_1588_TRIG_IN2 FTM3_CH2 GPIO4_06	In In Bidir Bidir	RGMII receive data 0 PTP trigger signal 2 FTM3 channel 2 input/output GPIO signal	
108	EC3_RX_CLK TSEC_1588_CLK_IN FTM3_QD_PHA GPIO4_07	In In In Bidir	RGMII receive clock PTP clock input FTM3 quad decoder phase A input GPIO signal	
101	EC3_RX_DV TSEC_1588_TRIG_IN1 FTM3_QD_PHB GPIO4_08	In In In Bidir	RGMII receive data valid PTP trigger signal 1 FTM3 quad decoder phase B input GPIO signal	

Table 5.16: RGMII EC3 signals

5.14 QUICC ENGINE

Quicc Engine in the LS1021A has two UCCs available. Features of this block are:

- UCC1 and UCC3
- TDMA and TDMB
- HDLC, UART, BISYNC on each UCC
- transparent protocol on each UCC; 1-bit (serial) data on UCC1, 1- and 4-bit data on UCC3.

Signals from QE block are available on the GPIO/LPC and I2S sections of the Qseven edge connector KE1. They are used for implementing native interfaces supported by QE or miscellaneous communication and industrial protocols that would benefit from offloading the work from main CPU to the QE. Borea is able to offer a custom QE microcode.

There are more interfaces available on the same pins as QE due to pinmuxing feature of the LS1021A. They are listed in the table below.

UCC1	UCC3
QE-UCC1	QE-UCC3
GPIO4(09:13,19:20)	GPIO4(14:18,21:22)
-	SPDIF
I2S_3	I2S_4
FTM4	FTM4
2D-ACE*	2D-ACE*

Table 5.17: Additional interfaces on QE pins

*: 2D-ACE interface is used for connecting CPU to the HDMI transmitter. This means that if HDMI is used, QE is not available!

Signals available on the QE UCC1 interface:

KE1 Pin	Signal	Direction	Function	Note
65	UCC1_RXD TDMA_RXD SAI3_RX_DATA FTM4_CH7 GPIO4_09	In In In Bidir Bidir	HDLC/UART receive data TDMA receive data I2S_3 receive data FTM4 channel 7 input/output GPIO	
63	UCC1_CTSB_RXDV TDMA_RSYNC SAI3_TX_BCLK FTM4_CH6 GPIO4_10	Out In Bidir Bidir Bidir	HDLC/UART Clear To Send TDMA receive frame sync I2S_3 transmit clock FTM4 channel 6 input/output GPIO	
67	UCC1_TXD TDMA_TXD SAI3_TX_DATA FTM4_CH5 GPIO4_11	Out Out Out Bidir Bidir	HDLC/UART transmit data TDMA transmit data I2S_3 transmit data FTM4 channel 5 input/output GPIO	
59	UCC1_RTSB_TXEN TDMA_TSYNC SAI3_TX_SYNC FTM4_CH4 GPIO4_12	In In Bidir Bidir Bidir	HDLC/UART Request To Send TDMA transmit frame sync I2S_3 transmit frame sync FTM4 channel 4 input/output GPIO	
185	UCC1_CDB_RXER TDMA_RQ EXT_AUDIO_MCLK1 FTM4_CH3 GPIO4_13	In Out In Bidir Bidir	HDLC/UART Carrier Detect TDMA request I2S audio master clock 1 FTM4 channel 3 input/output GPIO	
187	UCC1_CLK09 BRGO2 SAI3_RX_BCLK FTM4_QD_PHA GPIO4_19	In Out Bidir In Bidir	External QE input clock 9 Baud rate generator 2 output I2S_3 receive clock FTM4 quadrature decoder phase A input GPIO	
189	UCC1_CLK10 BRGO3 SAI3_RX_SYNC FTM4_QD_PHB GPIO4_20	In Out Bidir In Bidir	External QE input clock 10 Baud rate generator 3 output I2S_3 transmit frame sync FTM4 quadrature decoder phase B input GPIO	

Table 5.18: QE UCC1 signals

Signals of QE UCC3 interface:

KE1 Pin	Signal	Direction	Function	Note
195	UCC3_RXD TDMB_RXD SPDIF_IN SAI4_RX_DATA FTM4_CH2 GPIO4_14	In In In In Bidir Bidir	HDLC/UART receive data TDMB receive data SPDIF input data I2S_4 receive data FTM4 channel 2 input/output GPIO	
194	UCC3_CTSB_RXDV TDMB_RSYNC SPDIF_PLOCK SAI4_TX_BCLK FTM4_CH1 GPIO4_15	Out In Bidir Bidir Bidir Bidir	HDLC/UART Clear To Send TDMB receive frame sync SPDIF lock detection I2S_4 transmit clock FTM4 channel 1 input/output GPIO	
196	UCC3_TXD TDMB_TXD SPDIF_OUT SAI4_TX_DATA FTM4_CH0 GPIO4_16	Out Out Out Out Bidir Bidir	HDLC/UART transmit data TDMB transmit data SPDIF output data I2S_4 transmit data FTM4 channel 0 input/output GPIO	
186	UCC3_RTSB_TXEN TDMB_TSYNC SPDIF_SRCLK SAI4_TX_SYNC FTM4_FAULT GPIO4_17	Out In Bidir Bidir In Bidir	HDLC/UART Request To Send TDMB transmit frame sync SPDIF RX clock I2S_4 transmit frame sync FTM4 fault input GPIO	
188	UCC3_CDB_RXER TDMB_RQ SPDIF_EXTCLK SAI4_RX_BCLK FTM4_EXTCLK GPIO4_18	In Out Bidir Bidir Bidir Bidir	HDLC/UART Carrier Detect TDMB request SPDIF external clock I2S_4 receive clock FTM4 external clock GPIO	
190	UCC3_CLK11 BRGO4 SAI4_RX_SYNC FTM8_CH0 GPIO4_21	In Out Bidir Bidir Bidir	External QE input clock 11 Baud rate generator 4 output I2S_4 receive frame sync FTM8 channel 0 GPIO	
192	UCC3_CLK12 BRGO1 FTM8_CH1 GPIO4_22	In Out Bidir Bidir	External QE input clock 12 Baud rate generator 1 output FTM8 channel 1 GPIO	

Table 5.19: QE UCC3 signals

5.15 HDMI

Table shows signals of HDMI interface:

KE1 Pin	Signal	Direction	Function	Note
131	TMDS_CLK+	Out	HDMI positive clock	
133	TMDS_CLK-	Out	HDMI negative clock	
143	TMDS_L0+	Out	HDMI positive data 0	
145	TMDS_L0-	Out	HDMI negative data 0	
137	TMDS_L1+	Out	HDMI positive data 1	
139	TMDS_L1-	Out	HDMI negative data 1	
149	TMDS_L2+	Out	HDMI positive data 2	
151	TMDS_L2-	Out	HDMI negative data 2	
152	HDMI_CTRL_CLK	Out	DDC based clock signal for HDMI device.	
150	HDMI_CTRL_DAT	In	DDC based data signal for HDMI device.	
153	HDMI_HPD#	In	Hot plug detection	PD 10K

Table 5.20: HDMI signals

5.16 JTAG

JTAG interface is used for testing and debugging the CPU. It is available on the JTAG/MFG section of Qseven edge connector KE1 and debug connector J3.

Table shows signals of JTAG interface:

KE1 Pin	Signal	Direction	Function	Note
200	JTAG_TCK	In	JTAG clock	PU 10K, 1.8V
202	JTAG_TMS	In	JTAG mode	1.8V
203	JTAG_TDI	In	JTAG data in	1.8V
199	JTAG_TDO	Out	JTAG data out	1.8V
201	JTAG_TRST#	In	JTAG reset, active low	PU 1K, 1.8V

Table 5.21: JTAG signals

Caution: JTAG uses 1.8V logic levels.

6 CONNECTOR DETAILS

6.1 LOCATION OF CONNECTORS

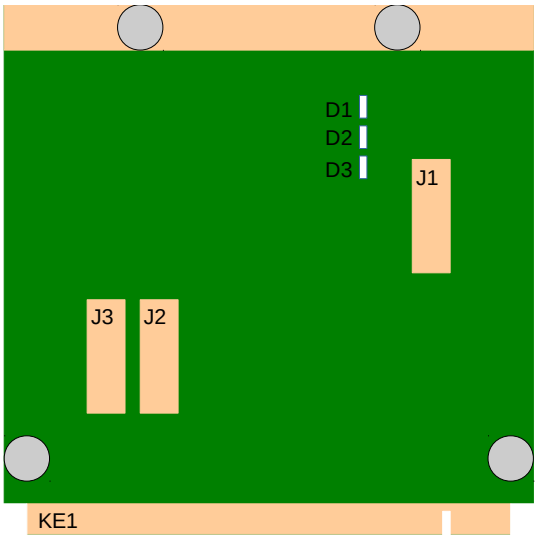

Illustration 6.1: Location of connectors

6.2 KE1: QSEVEN EDGE

Connector Type	230 pin edge connector
Connector Manufacturer	PCB
Mates to	Foxconn AS0B326-S78N-7F

Table 6.1: KE1 Qseven edge connector type

Pin	Signal	Direction	Pin	Signal	Direction
1	GND	-	2	GND	-
3	ETH_MDI3-	Bidir	4	ETH_MDI2-	Bidir
5	ETH_MDI3+	Bidir	6	ETH_MDI2+	Bidir
7	LINK100#	Out	8	LINK1000#	Out
9	ETH_MDI1-	Bidir	10	ETH_MDI0-	Bidir
11	ETH_MDI1+	Bidir	12	ETH_MDI0+	Bidir
13	NC	-	14	ACT#	Out
15	NC	-	16	NC	-
17	NC	-	18	SUS_S3#	Out
19	NC	-	20	PWRBTN#	In
21	SLP_BTN#	In	22	NC	-
23	GND	-	24	GND	-
KEY					

Pin	Signal	Direction	Pin	Signal	Direction
25	GND	-	26	PWGIN	In
27	NC	-	28	RSTBTN#	In
29	SATA_TX+	Out	30	NC	-
31	SATA_TX-	Out	32	NC	-
33	NC	-	34	GND	-
35	SATA_RX+	In	36	NC	-
37	SATA_RX-	In	38	NC	-
39	GND	-	40	GND	-
41	NC	-	42	SD_CLK	Out
43	SD_CD#	In	44	NC	-
45	SD_CMD	Out	46	SD_WP	In
47	NC	-	48	SD_DATA1	Bidir
49	SD_DATA0	Bidir	50	SD_DATA3	Bidir
51	SD_DATA2	Bidir	52	SD_DATA5	Bidir
53	SD_DATA4	Bidir	54	SD_DATA7	Bidir
55	SD_DATA6	Bidir	56	USB1_DRVBUS	Out
57	GND	-	58	GND	-
59	UCC1_RTSB_TXEN	Out	60	I2C1_SCL	Bidir
61	NC	-	62	I2C1_SDA	Bidir
63	UCC1_CTSB_RXDV	In	64	SMB_ALERT#	In
65	UCC1_RXD	In	66	I2C2_SCL	Bidir
67	UCC1_TXD	Out	68	I2C2_SDA	Bidir
69	NC	-	70	WDTRIG#	In
71	NC	-	72	WDOUT	Out
73	GND	-	74	GND	-
75	NC	-	76	NC	-
77	NC	-	78	NC	-
79	NC	-	80	NC	-
81	USB1_TX-	Out	82	USB1_RX-	In
83	USB1_TX+	Out	84	USB1_RX+	In
85	NC	-	86	USB1_PWRFAULT	In
87	NC	-	88	NC	-
89	NC	-	90	NC	-
91	USB1_VBUS	In	92	USB1_ID	Bidir
93	USB1_D-	Bidir	94	NC	-
95	USB1_D+	Bidir	96	NC	-
97	GND	-	98	GND	-
99	EC3_GTX_CLK125	In	100	EC3_RXD0	In
101	EC3_RX_DV	In	102	EC3_RXD1	In
103	EC3_TX_EN	Out	104	EC3_RXD2	In
105	EC3_GTX_CLK	Out	106	EC3_RXD3	In

Pin	Signal	Direction	Pin	Signal	Direction
107	EC3_TXD0	Out	108	EC3_RX_CLK	In
109	EC3_TXD1	Out	110	EC2_RX_DV	In
111	EC3_TXD2	Out	112	EC2_RXD0	In
113	EC3_TXD3	Out	114	EC2_RXD1	In
115	EC2_TX_EN	Out	116	EC2_RXD3	In
117	GND	-	118	GND	-
119	EC2_GTX_CLK	Out	120	NC	-
121	EC2_GTX_CLK125	In	122	NC	-
123	EC2_TXD0	Out	124	EC2_RX_CLK	In
125	EC2_TXD1	Out	126	MDIO_OUT	Bidir
127	EC2_TXD3	Out	128	MDC_OUT	Out
129	EC2_TXD2	Out	130	EC2_RXD2	In
131	TMDS_CLK+	Out	132	UART2_RTS#	Out
133	TMDS_CLK-	Out	134	UART2_CTS#	In
135	GND	-	136	GND	-
137	TMDS_L1+	Out	138	NC	-
139	TMDS_L1-	Out	140	NC	-
141	GND	-	142	GND	-
143	TMDS_L0+	Out	144	UART2_SOUT	Out
145	TMDS_L0-	Out	146	UART2_SIN	In
147	GND	-	148	GND	-
149	TMDS_L2+	Out	150	HDMI_CTRL_DAT	In
151	TMDS_L2-	Out	152	HDMI_CTRL_CLK	Out
153	HDMI_HPD#	In	154	NC	-
155	PCIE_CLK_REF+	Out	156	NC	-
157	PCIE_CLK_REF-	Out	158	PCIE_RST#	Out
159	GND	-	160	GND	-
161	PCIE3_TX+	Out	162	PCIE3_RX+	In
163	PCIE3_TX-	Out	164	PCIE3_RX-	In
165	GND	-	166	GND	-
167	PCIE2_TX+	Out	168	PCIE2_RX+	In
169	PCIE2_TX-	Out	170	PCIE2_RX-	In
171	UART1_SOUT	Out	172	UART1_RTS#	Out
173	PCIE1_TX+	Out	174	PCIE1_RX+	In
175	PCIE1_TX-	Out	176	PCIE1_RX-	In
177	UART1_SIN	In	178	UART1_CTS#	In
179	PCIE0_TX+	Out	180	PCIE0_RX+	In
181	PCIE0_TX-	Out	182	PCIE0_RX-	In
183	GND	-	184	GND	-
185	UCC1_CDB_RXER	In	186	UCC3_RTSB_TXEN	Out
187	UCC1_CLK09	In	188	UCC3_CDB_RXER	In

Pin	Signal	Direction	Pin	Signal	Direction
189	UCC1_CLK10	In	190	UCC3_CLK11	In
191	NC	-	192	UCC3_CLK12	In
193	NC	-	194	UCC3_CTSB_RXDV	In
195	UCC3_RXD	In	196	UCC3_TXD	Out
197	GND	-	198	GND	-
199	SPI_MOSI	Out	200	SPI_CS0#	Out
201	SPI_MISO	In	202	SPI_CS1#	Out
203	SPI_CLK	Out	204	JTAG_TRST#	In
205	NC	-	206	NC	-
207	JTAG_TCK	In	208	JTAG_TDI	In
209	JTAG_TDO	Out	210	JTAG_TMS	In
211	VCC	-	212	VCC	-
213	VCC	-	214	VCC	-
215	VCC	-	216	VCC	-
217	VCC	-	218	VCC	-
219	VCC	-	220	VCC	-
221	VCC	-	222	VCC	-
223	VCC	-	224	VCC	-
225	VCC	-	226	VCC	-
227	VCC	-	228	VCC	-
229	VCC	-	230	VCC	-

Table 6.2: KE1 Qseven edge connector pinout

6.3 J1: MCU DEBUG

Connector Type	TC2050-IDC
Connector Manufacturer	Tag-Connect

Table 6.3: J1 SWD debug connector type

Pin	Signal	Direction
1	+3.3V_PRE	-
2	SWD_CLK	In
3	-	-
4	RSTBTN#	In
5	GND	-
6	SUS_S3# (MCU UART_RX)	In
7	WDTRIG (MCU UART_TX)	Out
8	TEST1 (MCU free GPIO)	Bidir
9	MCU_RST#	In
10	SWD_DIO	Bidir

Table 6.4: J1 SWD debug connector pinout

6.4 J2: CPU FUSE PROGRAMMING POWER

Connector Type	TC2050-IDC
Connector Manufacturer	Tag-Connect

Table 6.5: J2 JTAG and UART debug connector type

Pin	Signal	Direction
1	PWR_PROG_SFP	Out
2	OVDD	In
3	OVDD	In
4	PWR_PROG_MTR	Out
5	-	-
6	-	-
7	VDD_FA_VDD	Out
8	VDD	In
9	VDD	In
10	VDD_LP	Out

Table 6.6: J2 JTAG and UART debug connector pinout

Connector is used to interface jumpers between 1-2, 3-4, 7-8 and 9-10 during fuse programming. For more information, see LS1021ARM [1].

6.5 J3: CPU DEBUG

Connector Type	TC2050-IDC
Connector Manufacturer	Tag-Connect

Table 6.7: J3 JTAG and UART debug connector type

Pin	Signal	Direction
1	OVDD (1.8V)	-
2	JTAG_TCK_18	In
3	JTAG_TMS_18	In
4	JTAG_POR#_18	In
5	GND	-
6	UART1_SIN	In
7	UART1_SOUT	Out
8	JTAG_TDO_18	Out
9	JTAG_TDI_18	In
10	JTAG_TRST#_18	In

Table 6.8: J3 JTAG and UART debug connector pinout

6.6 LEDS

Board comprises three LED indicators.

LED	Function during boot stage	Function during normal operation
D1	VCC power (+5V)	VCC power (+5V)
D2	Boot unsuccessful	Application specific, controllable with CPU
D3	Boot unsuccessful	Application specific, controllable with CPU

Table 6.9: LED indicators

7 ELECTRICAL SPECIFICATION

7.1 DC ELECTRICAL CHARACTERISTICS

7.1.1 2.5V I/O POWER SUPPLY ON LVDS GPIOS

Parameter	Symbol	Min	Max	Unit	Note
Board supply voltage	VDD	4.75V	5.25V	V	Typ. 5V
Input pin high voltage	VIH	0.7 * LVDD	-	V	LVDD = 2.5V
Input pin low voltage	VIL	-	0.2 * LVDD	V	LVDD = 2.5V
Input pin current (VIN = 0V or VIN = LVDD)	IIN	-	±50	µA	
Output pin high voltage (LVDD = min, IOL = -1mA)	VOH	2.0	-	V	
Output pin low voltage (LVDD = min, IOL = 1mA)	VOL	-	0.4	V	
Output pin current	IOUT	-	±1	mA	

Table 7.1: DC electrical characteristics

7.1.2 3.3V I/O POWER SUPPLY ON LVDS GPIOS

Parameter	Symbol	Min	Max	Unit	Note
Board supply voltage	VDD	4.75V	5.25V	V	Typ. 5V
Input pin high voltage	VIH	0.7 * LVDD	-	V	LVDD = 3.3V
Input pin low voltage	VIL	-	0.2 * LVDD	V	LVDD = 3.3V
Input pin current (VIN = 0V or VIN = LVDD)	IIN	-	±50	µA	
Output pin high voltage (LVDD = min, IOL = -2mA)	VOH	2.4	-	V	
Output pin low voltage (LVDD = min, IOL = 2mA)	VOL	-	0.4	V	
Output pin current	IOUT	-	±2	mA	

Table 7.2: DC electrical characteristics

7.2 AC ELECTRICAL CHARACTERISTICS

Consult data sheet of LS1021A CPU [2].

7.3 POWER CONSUMPTION

Power mode	VDD	Typical	Max	Note
Active	5V	*	1.5 A	
Standby	5V	-	TBD	

Table 7.3: Power consumption

* Typical consumption heavily depends on usage case. For example: RakunLS1, boot from SD card, 1x 1000BaseT, 25 degC environment, Linux shell consumes 0.8A. Heavy CPU processing 0.95A.

8 MECHANICAL SPECIFICATION

RakunLS1 module outline and mechanical dimensions comply with Qseven specification 2.0 [3].

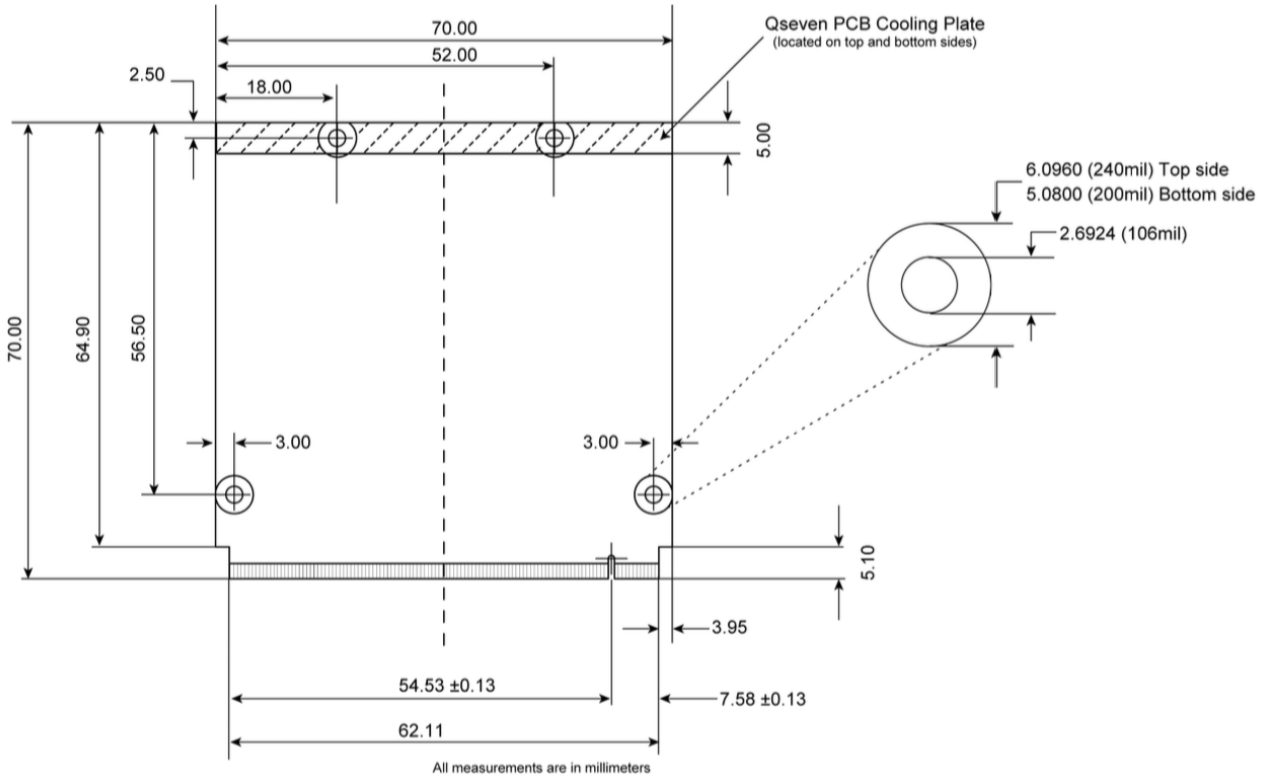

Illustration 8.1: Mechanical outline

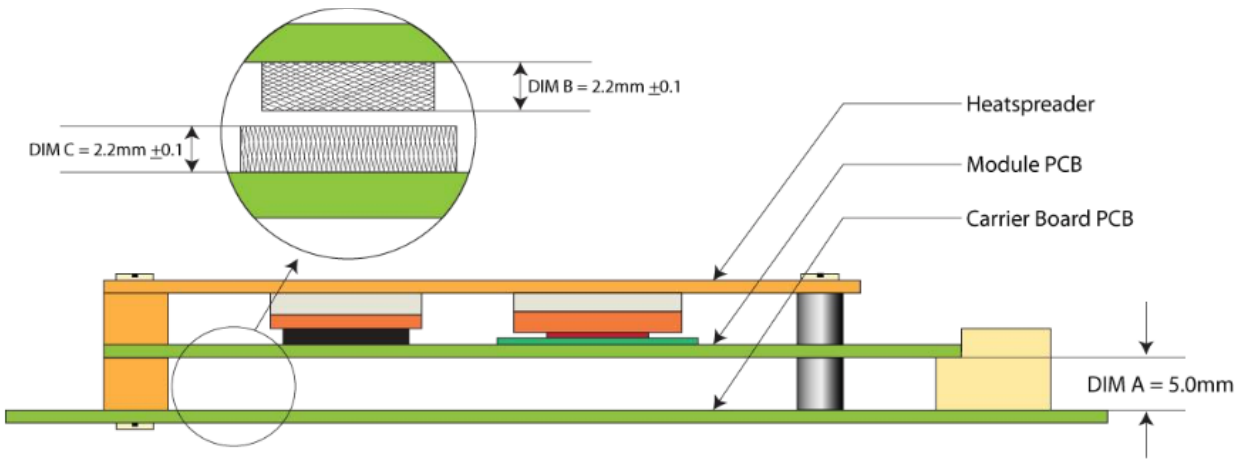

Illustration 8.2: Component heights

9 REFERENCE DOCUMENTS

1. QorIQ LS1021A Reference Manual, LS1021ARM, Rev. E, 01/2015, NXP
2. QorIQ LS1021A Data Sheet, LS1021A, Rev F, 11/2014, NXP
3. Qseven Specification 2.0, Rev. 2.0, 09/2012, with errata E2.0-001, 07/2013, SGET

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